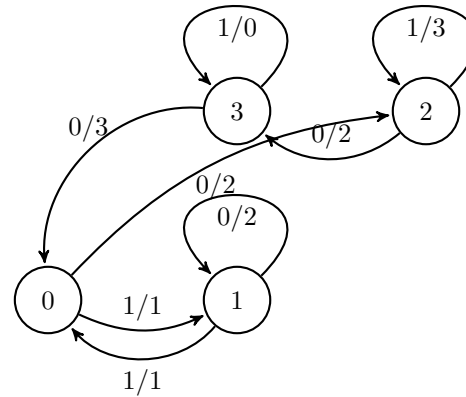


1 Zustandsdiagramm



2 Zustandstabelle

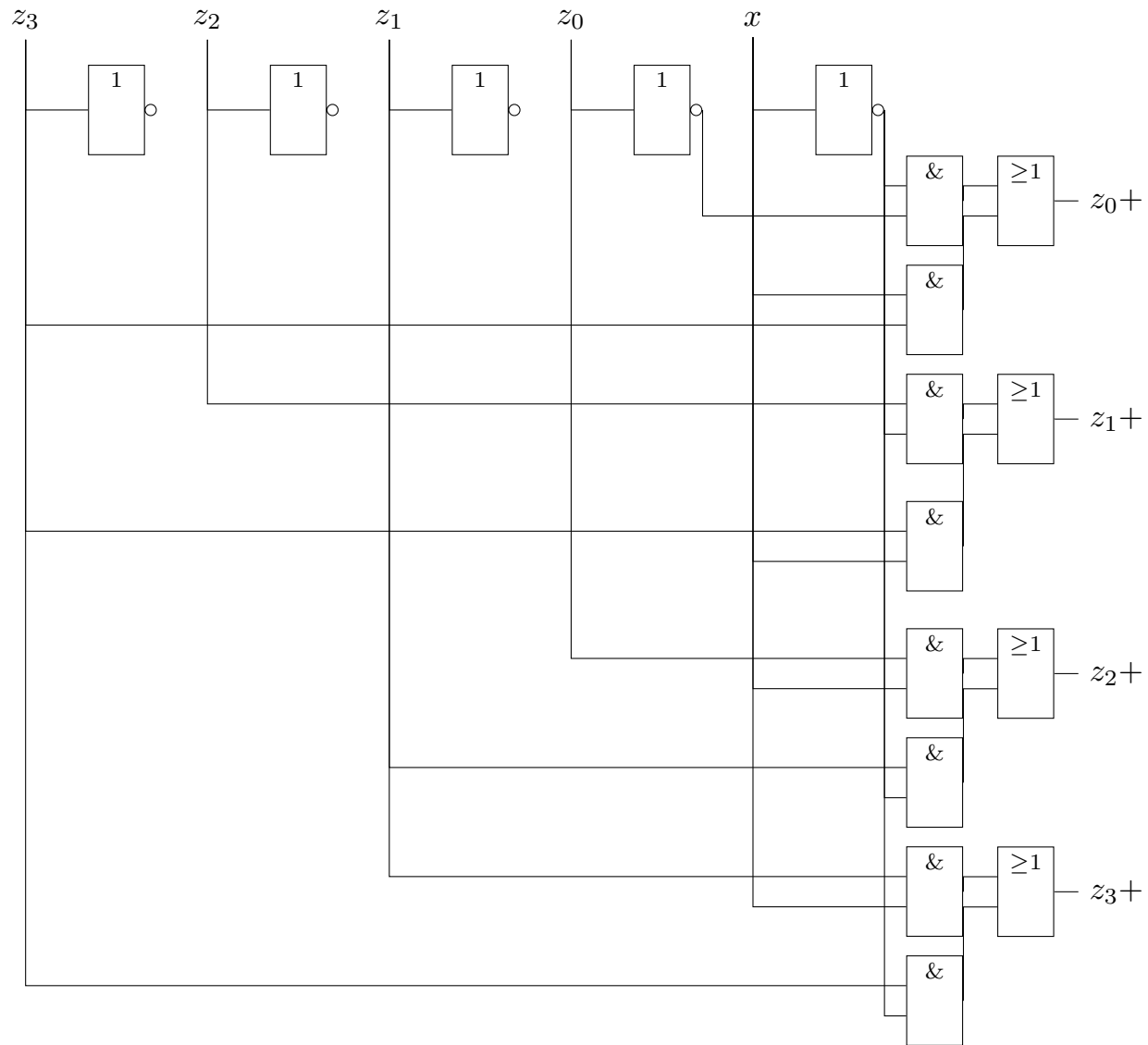
| Zustand | Eingabe | Ausgabe | Folgezustand | z3+ | z2+ | z1+ | z0+ |
|---------|---------|---------|--------------|-----|-----|-----|-----|
| 0 | 0 | 2 | 2 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 2 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 2 | 3 | 1 | 0 | 0 | 0 |
| 2 | 1 | 3 | 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 3 | 0 | 0 | 0 | 0 | 1 |
| 3 | 1 | 0 | 3 | 1 | 0 | 0 | 0 |

3 Funktionsgleichung

$$\begin{aligned}
 z3+ &:= (z2 \text{ and not } x) \text{ or } (z3 \text{ and } x) \\
 z2+ &:= (z0 \text{ and not } x) \text{ or } (z2 \text{ and } x) \\
 z1+ &:= (z0 \text{ and } x) \text{ or } (z1 \text{ and not } x) \\
 z0+ &:= (z1 \text{ and } x) \text{ or } (z3 \text{ and not } x)
 \end{aligned}$$

```
y1 := (z0 and not x) or  
      (z1 and not x) or  
      (z2 and not x) or  
      (z2 and x) or  
      (z3 and not x)  
y0 := (z0 and x) or  
      (z1 and x) or  
      (z2 and x) or  
      (3 and not x)
```

4 Schaltplan Übergangsschaltnetz



5 VHDL-Code

```
library ieee;
use ieee.std_logic_1164.all;

entity automat20240125 is
port (
    z3, z2, z1, z0: in std_logic;
    x: in std_logic;
    y1, y0: out std_logic;
    z3s, z2s, z1s, z0s: out std_logic
);
end;

architecture behaviour of automat20240125 is
begin
    z3s <= (z2 and not x) or (z3 and x);
    z2s <= (z0 and not x) or (z2 and x);
    z1s <= (z0 and x) or (z1 and not x);
    z0s <= (z1 and x) or (z3 and not x);
    y1 <= (z0 and not x) or
        (z1 and not x) or
        (z2 and not x) or
        (z2 and x) or
        (z3 and not x);
    y0 <= (z0 and x) or
        (z1 and x) or
        (z2 and x) or
        (z3 and not x);
end;

library ieee;
use ieee.std_logic_1164.all;

entity automat20240125testbench is
port (
```

```

    z3, z2, z1, z0: inout std_logic;
    x: inout std_logic;
    y1, y0: inout std_logic;
    z3s, z2s, z1s, z0s: inout std_logic
);
end;

architecture behaviour of automat20240125testbench is
    component automat20240125
        port (
            z3, z2, z1, z0: in std_logic;
            x: in std_logic;
            y1, y0: out std_logic;
            z3s, z2s, z1s, z0s: out std_logic
        );
    end component;
begin
    sn: automat20240125 PORT MAP (z3=>z3, z2=>z2, z1=>z1, z0=>z0, x=>x, y1=>y1, y0=>y0,
        z3s=>z3s, z2s=>z2s, z1s=>z1s, z0s=>z0s);

    z0 <= '1' after 0 ns, '0' after 20 ns;
    z1 <= '0' after 0 ns, '1' after 20 ns, '0' after 40 ns;
    z2 <= '0' after 0 ns, '1' after 40 ns, '0' after 60 ns;
    z3 <= '0' after 0 ns, '1' after 60 ns, '0' after 80 ns;
    x <= '0' after 0 ns, '1' after 10 ns, '0' after 20 ns, '1' after 30 ns, '0'
        after 40 ns, '1' after 50 ns, '0' after 60 ns, '1' after 70 ns, '0' after 80 ns;

end;

```

6 GTKWave

